REMARKS

Applicant has amended claims 1-4. Applicant respectfully submits that the amendments to the claims are supported by the application as originally filed and do not contain any new matter. Accordingly, the Final Office Action will be discussed in terms of the claims as amended.

The Examiner has objected to claim 3 and pointed out a typographical error. Applicant has amended the typographical error in claim 3 and respectfully requests that the Examiner withdraw the objection.

The Examiner has stated that the IDS filed August 19, 2002 fails to comply with 37 CFR 1.98(a)(1) because it does not contain a list. In reply thereto, Applicant respectfully submits that the IDS mailed July 18, 2002 is in fact a list in that it does list Japanese Patent Application Laid Open No. H11-088052. In addition, Applicant respectfully submits that this prior art was in fact filed under 37 CFR 1.98(c) and is merely cumulative since it was cited by the Japanese Patent Office against application upon which priority was claimed and the corresponding Japanese application was allowed thereover. Notwithstanding the above, submitted herewith is a Form 1449 for the file.

The Examiner has rejected claims 1, 2 and 4 under 35 USC 102 as being anticipated by Ochiai et al., stating that Ochiai et al. discloses an integrated piezoelectric oscillator with amplifier 13, resonator 17 and divisional capacitors 15, 18.

In reply thereto, Applicant would like to point out that while Ochiai et al. may disclose an integrated piezoelectric oscillator with amplifier 13 and resonator 17 and divisional capacitors 15, 18, the control voltage is within the range of –V to +V with zero volts in between, as is clearly shown in Fig. 3(b) of Ochiai et al. In contrast thereto, in Applicant's invention, in order to secure a control voltage that has a sufficiently wide range of polarity, either plus or minus, the MOS construction type capacitance element 3 is, as seen for instance in Fig. 1 of Applicant's application, connected to ground via capacitors C1 and C3, thus obtaining a control voltage that is either positive or negative. Still further, Applicant respectfully submits that in Ochiai et al. the MOS construction capacitor 14 is directly connected to VDD or to ground since VDD is an alternating current and thus is the same as ground. Accordingly, Applicant respectfully submits that the structure of Ochiai et al. is entirely different from Applicant's invention as claimed and

does not disclose that the MOS construction type capacitance element 3 would be connected to ground with a capacitor in between.

In view of the above, therefore, Applicant respectfully submits that Ochiai et al. does not disclose each and every element of Applicant's invention and claims 1, 2 and 4 are not anticipated by Ochiai et al.

In addition and in accordance with the Brief Description of the Drawings, Applicant has amended the drawings to indicate that Figs. 6-9 are prior art by way of an attached Letter to the Chief Draftsperson.

In view of the above, therefore, it is respectfully requested that this Rule 116 Amendment be entered, favorably considered and the case passed to issue.

Please charge any additional costs incurred by or in order to implement this Amendment or required by any requests for extensions of time to KODA & ANDROLIA DEPOSIT ACCOUNT NO. 11-1445.

Respectfully submitted,

KODA & ANDROLIA

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Name

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